



## TE0808 StarterKit

Revision v.55

Exported on 2023-05-17

Online version of this document:

<https://wiki.trenz-electronic.de/display/PD/TE0808+StarterKit>

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## 4 Overview

Linux with basic periphery of TE0808 StarterKit (TEBF0808 Carrier).

Refer to <http://trenz.org/te0808-info> for the current online version of this manual and other available documentation.

### 4.1 Key Features

- Vitis/Vivado 2021.2.1
- TEBF0808
- Linux
- USB
- ETH
- MAC from EEPROM
- PCIe
- SATA
- SD
- I2C
- RGPIIO
- Display Port (DP)
- user LED access

### 4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2023-04-13	2021.2.1	TE0808-StarterKit-vivado_2021.2-build_20_20230413092755.zip TE0808-StarterKit_noprebuilt-vivado_2021.2-build_20_20230413092755.zip	Manuela Strücker	<ul style="list-style-type: none"> <li>• new assembly variants</li> </ul>
2022-09-29	2021.2.1	TE0808-StarterKit-vivado_2021.2-build_17_20220929082218.zip TE0808-StarterKit_noprebuilt-vivado_2021.2-build_17_20220929082218.zip	Manuela Strücker	<ul style="list-style-type: none"> <li>• script update</li> <li>• new assembly variants</li> </ul>
2022-09-12	2021.2.1	TE0808-StarterKit-vivado_2021.2-build_15_20220912090625.zip TE0808-StarterKit_noprebuilt-	Manuela Strücker	<ul style="list-style-type: none"> <li>• update board part files compatible to Vivado 2021.2.1</li> </ul>

<b>Date</b>	<b>Vivado</b>	<b>Project Built</b>	<b>Authors</b>	<b>Description</b>
		vivado_2021.2-build_15_20220912090625.zip		
2022-03-16	2021.2	TE0808-StarterKit-vivado_2021.2-build_11_20220316082848.zip TE0808-StarterKit_noprebuilt-vivado_2021.2-build_11_20220316082848.zip	Manuela Strücker	<ul style="list-style-type: none"> <li>• 2021.2 release</li> <li>• update board files</li> </ul>
2021-05-12	2020.2	TE0808-StarterKit-vivado_2020.2-build_5_20210512133800.zip TE0808-StarterKit_noprebuilt-vivado_2020.2-build_5_20210512133822.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• update board files</li> <li>• boot.scr update to version1 → image.ub on sd, eMMC, USB possible</li> </ul>
2021-02-05	2020.2	TE0808-StarterKit-vivado_2020.2-build_1_20210205120058.zip TE0808-StarterKit_noprebuilt-vivado_2020.2-build_1_20210205120122.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• bugfix init.sh script usage</li> </ul>
2021-02-05	2020.2	TE0808-StarterKit_noprebuilt-vivado_2020.2-build_1_20210204142828.zip TE0808-StarterKit-vivado_2020.2-build_1_20210204142713.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• 2020.2 update</li> <li>• add boot.scr file</li> <li>• device tree has change</li> <li>• petalinux fsbl patch (betaversion)</li> </ul>
2020-09-29	2019.2	TE0808-StarterKit_noprebuilt-vivado_2019.2-build_15_20200928195324.zip TE0808-StarterKit-vivado_2019.2-build_15_20200928195304.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• bugfix 8GB board part files</li> </ul>
2020-09-22	2019.2	TE0808-StarterKit_noprebuilt-vivado_2019.2-build_14_20200922071643.zip TE0808-StarterKit-vivado_2019.2-build_14_20200922071704.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variants</li> </ul>



<b>Date</b>	<b>Vivado</b>	<b>Project Built</b>	<b>Authors</b>	<b>Description</b>
2020-03-25	2019.2	TE0808-StarterKit_noprebuilt-vivado_2019.2-build_8_20200325083508.zip TE0808-StarterKit-vivado_2019.2-build_8_20200325083436.zip	John Hartfiel	<ul style="list-style-type: none"> <li>script update</li> </ul>
2020-01-22	2019.2	TE0808-StarterKit_noprebuilt-vivado_2019.2-build_3_20200122142340.zip TE0808-StarterKit-vivado_2019.2-build_3_20200122142318.zip	John Hartfiel	<ul style="list-style-type: none"> <li>2019.2 update</li> <li>Vitis support</li> <li>FSBL SI programming procedure update</li> <li>petalinux device tree and u-boot update</li> </ul>
2019-08-09	2018.3	TE0808-StarterKit_noprebuilt-vivado_2018.3-build_07_20190809131638.zip TE0808-StarterKit-vivado_2018.3-build_07_20190809131620.zip	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variants</li> <li>small fsbl update(supports all GTR disabled now)</li> </ul>
2019-05-07	2018.3	TE0808-StarterKit_noprebuilt-vivado_2018.3-build_05_20190507124429.zip TE0808-StarterKit-vivado_2018.3-build_05_20190507124418.zip	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variant</li> <li>TE Script update</li> <li>rework of the FSBLs</li> <li>some additional Linux features</li> <li>MAC from EEPROM</li> <li>new assembly variants</li> <li>remove special compiler flags, which was needed in 2018.2</li> </ul>
2018-07-11	2018.2	TE0808-StarterKit_noprebuilt-vivado_2018.2-build_02_20180711091558.zip TE0808-StarterKit-vivado_2018.2-build_02_20180711091049.zip	John Hartfiel	<ul style="list-style-type: none"> <li>small petalinux changes</li> <li>IO renaming</li> <li>PL Design changes</li> <li>additional notes for FSBL generated with Win SDK</li> <li>changed *.bif</li> </ul>
2018-05-24	2017.4	TE0808-StarterKit_noprebuilt-vivado_2017.4-build_10_20180524091231.zip TE0808-StarterKit-vivado_2017.4-build_10_20180524091208.zip	John Hartfiel	<ul style="list-style-type: none"> <li>solved Linux flash issue</li> </ul>

<b>Date</b>	<b>Vivado</b>	<b>Project Built</b>	<b>Authors</b>	<b>Description</b>
2018-03-29	2017.4	TE0808-StarterKit_noprebuilt-vivado_2017.4-build_07_20180329145308.zip TE0808-StarterKit-vivado_2017.4-build_07_20180329145246.zip	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variant</li> </ul>
2018-02-06	2017.4	TE0808-StarterKit_noprebuilt-vivado_2017.4-build_05_20180206082740.zip TE0808-StarterKit-vivado_2017.4-build_05_20180206082722.zip	John Hartfiel	<ul style="list-style-type: none"> <li>same clk for both VIO</li> </ul>
2018-02-05	2017.4	TE0808-StarterKit_noprebuilt-vivado_2017.4-build_05_20180205083231.zip TE0808-StarterKit-vivado_2017.4-build_05_20180205083208.zip	John Hartfiel	<ul style="list-style-type: none"> <li>solved JTAG/Linux problem</li> </ul>
2018-01-17	2017.4	TE0808-StarterKit-vivado_2017.4-build_05_20180117094213.zip TE0808-StarterKit_noprebuilt-vivado_2017.4-build_05_20180117094231.zip	John Hartfiel	<ul style="list-style-type: none"> <li>solved USB problem</li> <li>small board part update</li> </ul>
2018-01-15	2017.4	TE0808-StarterKit-vivado_2017.4-build_03_20180115092306.zip TE0808-StarterKit_noprebuilt-vivado_2017.4-build_03_20180115092511.zip	John Hartfiel	<ul style="list-style-type: none"> <li>rework board part files</li> <li>rework design</li> </ul>
2017-12-18	2017.2	TE0808-StarterKit_noprebuilt-vivado_2017.2-build_07_20171219151749.zip TE0808-StarterKit-vivado_2017.2-build_07_20171219151728.zip	John Hartfiel	<ul style="list-style-type: none"> <li>initial release</li> </ul>

**Table 1: Design Revision History**

## 4.3 Release Notes and Know Issues

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Issues	Description	Workaround/Solution	To be fixed version
Xilinx Software	Incompatibility of board files for ZynqMP with eMMC activated between 2021.2 and 2021.2.1 patch, see <a href="#">Xilinx Forum Request<sup>1</sup></a>	use corresponding board files for the Vivado versions	--
MAC from EEPROM	The MAC address stored in the EEPROM is not read out and initialised correctly during start-up. This is caused by two I2C expanders each switched to the same EEPROM with the same address i2cswitch@73 --> i2c@5 --> reg = <0x50> and i2cswitch@77 --> i2c@4 --> reg = <0x50>	Switching the second I2C expander (i2cswitch@77) to another channel in the fsbl solves the error during the start-up procedure.	<b>Solved</b> with 20220316 update
QSPI Flash	Flash programming is not supported with boot mode QSPI or SD.	If flash programming fails, configure device for JTAG boot mode and try again or use older Vivado Versions for programming. (Vivado 2020.2 or 2019.2)	--
Flash access on Linux	Device tree is not correct on Linux	add compatibility to "compatible "jedec,spi-nor""	<b>Solved</b> with 20180524 update
USB UART Terminal is blocked/ SDK Debugging is blocked	This happens only with 2017.4 Linux, when JTAG connection is	Do not use HW Manager connection, or if debugging is necessary:	<b>Solved</b> with 20180205 update

<sup>1</sup> [https://support.xilinx.com/s/feed/0D54U00005Wbon6SAB?language=en\\_US](https://support.xilinx.com/s/feed/0D54U00005Wbon6SAB?language=en_US)

Issues	Description	Workaround/Solution	To be fixed version
	established on Vivado HW Manager.	<ol style="list-style-type: none"> <li>1. Boot linux with usb terminal</li> <li>2. From the terminal: root root mount ifconfig eth0</li> <li>3. Open two new SSH terminals via ethernet: root root , run user application ...</li> <li>4. Exit and close the usb terminal</li> </ol>	

**Table 2: Known Issues**

## 4.4 Requirements

### 4.4.1 Software

Software	Version	Note
Vitis	2021.2.1	needed, Vivado is included into Vitis installation
PetaLinux	2021.2	needed
SI ClockBuilder Pro	---	optional

**Table 3: Software**

### 4.4.2 Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).<sup>2</sup>

Complete List is available on "<project folder>\board\_files\\*\_board\_files.csv"

Design supports following modules:

<sup>2</sup> <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
<del>TE0808-ES1</del>	es1_2gb	REV03  REV02	2GB	64MB	NA	NA	Not longer supported by vivado
<del>TE0808-ES2</del>	es2_2gb	REV04  REV03	2GB	64MB	NA	NA	Not longer supported by vivado
<del>TE0808-2ES2</del>	2es2_2gb	REV04  REV03	2GB	64MB	NA	NA	Not longer supported by vivado
TE0808-04-09EG-1EA	9eg_1e_2gb	REV04	2GB	64MB	NA	NA	NA
TE0808-04-09EG-1EB	9eg_1e_4gb	REV04	4GB	64MB	NA	NA	NA
TE0808-04-09EG-1ED	9eg_1e_4gb	REV04	4GB	64MB	NA	1 mm connectors	NA
TE0808-04-09EG-2IB	9eg_2i_4gb	REV04	4GB	64MB	NA	NA	NA
TE0808-04-15EG-1EB	15eg_1e_4gb	REV04	4GB	64MB	NA	NA	NA
TE0808-04-09EG-1EE	9eg_1e_4gb	REV04	4GB	128MB	NA	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0808-04-09EG-1EL	9eg_1e_4gb	REV04	4GB	128 MB	NA	1 mm connectors	NA
TE0808-04-09EG-2IE*	9eg_2i_4gb	REV04	4GB	128 MB	NA	NA	NA
TE0808-04-15EG-1EE	15eg_1e_4gb	REV04	4GB	128 MB	NA	NA	NA
TE0808-04-06EG-1EE	6eg_1e_4gb	REV04	4GB	128 MB	NA	NA	NA
TE0808-04-06EG-1E3	6eg_1e_4gb	REV04	4GB	128 MB	NA	1 mm connectors	NA
TE0808-04-6GI21-L	6eg_2i_4gb	REV04	4GB	128 MB	NA	1 mm connectors	NA
TE0808-04-6BI21-A	6eg_1i_4gb	REV04	4GB	128 MB	NA	NA	NA
TE0808-04-9GI21-A	9eg_2i_4gb	REV04	4GB	128 MB	NA	NA	NA
TE0808-04-9BE21-A	9eg_1e_4gb	REV04	4GB	128 MB	NA	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0808-04-6BE21-L	6eg_1e_4gb	REV04	4GB	128 MB	NA	1 mm connectors	NA
TE0808-04-6BE21-A	6eg_1e_4gb	REV04	4GB	128 MB	NA	NA	NA
TE0808-04-9BE21-L	9eg_1e_4gb	REV04	4GB	128 MB	NA	1 mm connectors	NA
TE0808-04-BBE21-A	15eg_1e_4gb	REV04	4GB	128 MB	NA	NA	NA
TE0808-04-6BI21-X	6eg_1i_4gb	REV04	4GB	128 MB	NA	NA	U41 replaced with schottky diodes
TE0808-05-6BE21-L	6eg_1e_4gb	REV05	4GB	128 MB	NA	1 mm connectors	NA
TE0808-05-6BE21-A	6eg_1e_4gb	REV05	4GB	128 MB	NA	NA	NA
TE0808-05-6BI21-D	6eg_1i_4gb	REV05	4GB	128 MB	NA	1 mm connectors	SoC without encryption
TE0808-05-6BI21-X	6eg_1i_4gb	REV05	4GB	128 MB	NA	NA	U41 replaced with schottky diodes

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0808-05-6BI41-X	6eg_1i_8gb	REV05	8GB	128 MB	NA	NA	U41 replaced with schottky diodes
TE0808-05-9BE21-A	9eg_1e_4gb	REV05	4GB	128 MB	NA	NA	NA
TE0808-05-9BE21-L	9eg_1e_4gb	REV05	4GB	128 MB	NA	1 mm connectors	NA
TE0808-05-9BI41-X	9eg_1i_8gb	REV05	8GB	128 MB	NA	NA	U41 replaced with schottky diodes
TE0808-05-9GI21-A	9eg_2i_4gb	REV05	4GB	128 MB	NA	NA	NA
TE0808-05-9GI21-C	9eg_2i_4gb	REV05	4GB	128 MB	NA	NA	SoC without encryption
TE0808-05-BBE21-A	15eg_1e_4gb	REV05	4GB	128 MB	NA	NA	NA
TE0808-05-BBE21-L	15eg_1e_4gb	REV05	4GB	128 MB	NA	1 mm connectors	NA
TE0808-05-S002	15eg_1e_4gb	REV05	4GB	128 MB	NA	NA	CAO
TE0808-05-S003	15eg_1e_4gb	REV05	4GB	128 MB	NA	NA	CAO



Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0808-05-S005	9eg_2i_4gb	REV05	4GB	128 MB	NA	NA	CAO
TE0808-05-S004	9eg_2i_4gb	REV05	4GB	128 MB	NA	NA	CAO
TE0808-05-6BE21-AK	6eg_1e_4gb	REV05	4GB	128 MB	NA	NA	NA
TE0808-05-9BE21-LK	9eg_1e_4gb	REV05	4GB	128 MB	NA	1 mm connectors	NA
TE0808-05-9GI21-AK	9eg_2i_4gb	REV05	4GB	128 MB	NA	NA	NA
TE0808-05-BBE21-AK	15eg_1e_4gb	REV05	4GB	128 MB	NA	NA	NA
TE0808-05-S006	9eg_2i_4gb	REV05	4GB	128 MB	NA	NA	CAO
TE0808-05-S016	9eg_1e_4gb	REV05	4GB	128 MB	NA	NA	CAO
TE0808-05-S018	9eg_2e_4gb	REV05	4GB	128 MB	NA	NA	CAO
TE0808-05-S019	9eg_2e_4gb	REV05	4GB	128 MB	NA	NA	CAO
TE0808-05-S021	9eg_2i_4gb	REV05	4GB	128 MB	NA	NA	CAO
TE0808-05-S022	6cg_1e_4gb	REV05	4GB	128 MB	NA	NA	CAO

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0808-05-S026	9eg_2i_4gb	REV05	4GB	128 MB	NA	CAO	CAO: without PLL
TE0808-05-9BE21-KZ	9eg_1e_4gb	REV05	4GB	128 MB	NA	1 mm connectors	NA
TE0808-05-9BE21-LZ	9eg_1e_4gb	REV05	4GB	128 MB	NA	1 mm connectors	NA
TE0808-05-9BE21-AK	9eg_1e_4gb	REV05	4GB	128 MB	NA	1 mm connectors	NA
TE0808-05-9BE21-AZ	9eg_1e_4gb	REV05	4GB	128 MB	NA	1 mm connectors	NA
TE0808-05-9GI21-AZ	9eg_2i_4gb	REV05	4GB	128 MB	NA	NA	NA
TE0808-05-BBE21-AZ	15eg_1e_4gb	REV05	4GB	128 MB	NA	NA	NA
TE0808-05-9BE81-A	9eg_1e_4gb	REV05	4GB	128 MB	NA	NA	NA
TE0808-05-S001	9eg_1e_8gb_D	REV05	8GB	128 MB	NA	CAO	CAO;Single Die DDR
TE0808-05-S020	9eg_2i_4gb	REV05	4GB	128 MB	NA	CAO	CAO
TE0808-05-S025	6eg_1e_4gb_D	REV05	4GB	128 MB	NA	CAO	CAO

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0808-05-S027	9eg_2i_4gb	REV05	4GB	128 MB	NA	CAO	CAO
TE0808-05-S029	9eg_2i_4gb	REV05	4GB	128 MB	NA	CAO	CAO
TE0808-05-S035	15eg_1e_4gb	REV05	4GB	128 MB	NA	CAO	CAO
TE0808-05-S036	15eg_1e_4gb	REV05	4GB	128 MB	NA	CAO	CAO
TE0808-05-S038	9eg_1e_4gb	REV05	4GB	128 MB	NA	CAO	CAO
TE0808-05-S039	6eg_1e_4gb	REV05	4GB	128 MB	NA	CAO	CAO: without PLL
TE0808-05-9GI21-KZ	9eg_2i_4gb	REV05	4GB	128 MB	NA	CAO	CAO
TE0808-05-S041	6eg_1e_4gb_D	REV05	4GB	128 MB	NA	CAO	CAO

**Table 4: Hardware Modules**

\*used as reference

Note: Design contains also Board Part Files for TE0808 only configuration, this board part files are not used for this reference design.

Design supports following carriers:

Carrier Model	Notes
TEBF0808*	Used as reference carrier. <b>Important:</b> CPLD Firmware REV07 or newer is recommended

**Table 5: Hardware Carrier**

\*used as reference

Additional HW Requirements:

Additional Hardware	Notes
Display Port Monitor	Optional HW Not all monitors are supported, also Adapter to other Standard can make trouble. Design was tested with <b>DELL U2412M</b>
USB Keyboard	Optional HW Can be used to get access to console which is show on Display Port
USB Stick	Optional HW USB was tested with USB memory stick
SATA Disk	Optional HW
PCIe Card	Optional HW
ETH cable	Optional HW Ethernet works with DHCP, but can be setup also manually
SD card	with fat32 partition

**Table 6: Additional Hardware**

\*used as reference

## 4.5 Content

For general structure and of the reference design, see [Project Delivery - Xilinx devices](#)<sup>3</sup>

### 4.5.1 Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints	Vivado Project will be generated by TE Scripts

<sup>3</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

Type	Location	Notes
	<project folder>\ip_lib <project folder>\board_files	
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<project folder>\os\petalinux	PetaLinux template with current configuration

**Table 7: Design sources**

#### 4.5.2 Additional Sources

Type	Location	Notes
SI5345	<project folder>/misc/PLL/SI5345_B	SI5345 Project with current PLL Configuration
init.sh	<project folder>/misc/sd/	Additional initialization script for Linux

**Table 8: Additional design sources**

#### 4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File

File	File-Extension	Description
Boot Script-File	*.scr	Distro Boot Script file
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Device Tree	*.dts	Device tree (2 possible, one for u-boot and one for linux)
Hardware-Platform-Description-File	*.xsa	Exported Vivado <a href="#">hardware description file</a> for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

**Table 9: Prebuilt files (only on ZIP with prebuilt content)**

#### 4.5.4 Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0808 "StarterKit" Reference Design](#)<sup>4</sup>

<sup>4</sup> [https://shop.trenz-electronic.de/Download/?path=Trenz\\_Electronic/Modules\\_and\\_Module\\_Carriers/5.2x7.6/TE0808/Reference\\_Design/2021.2/StarterKit](https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0808/Reference_Design/2021.2/StarterKit)

## 5 Design Flow

**⚠** Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- [AMD Development Tools](#)<sup>5</sup>
- [Vivado Projects - TE Reference Design](#)<sup>6</sup>
- [Project Delivery](#).<sup>7</sup>

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "\_create\_win\_setup.cmd" on Windows OS and "\_create\_linux\_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)<sup>8</sup>

**⚠ Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run \_create\_win\_setup.cmd/\_create\_linux\_setup.sh and follow instructions on shell:

### \_create\_win\_setup.cmd/\_create\_linux\_setup.sh

```
-----Set design paths-----
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
-----
-----TE Reference Design-----
-----
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
-----
Select (ex.: '0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.


<sup>5</sup> <https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDDevelopmentTools-XilinxSoftware-BasicUserGuides>

<sup>6</sup> <https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design>

<sup>7</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

<sup>8</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality>


- optional for manual changes: Select correct device and Xilinx install path on "design\_basic\_settings.cmd" and create Vivado project with "vivado\_create\_project\_gui mode.cmd"

 Note: Select correct one, see also [Vivado Board Part Flow](#)<sup>9</sup>  
**Important:** Use Board Part Files, which ends with \*\_tebf0808


4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

**run on Vivado TCL (Script generates design and export files into "\prebuilt\hardware\")**

```
\prebuilt\hardware\")">
TE::hw_build_design -export_prebuilt
```

 Using Vivado GUI is the same, except file export to prebuilt folder.


5. Create and configure your PetaLinux project with exported .xsa-file, see [PetaLinux KICKstart](#)<sup>10</sup>
  - use TE Template from "<project folder>\os\petalinux"
  - use exported .xsa file from "<project folder>\prebuilt\hardware<short name>". **Note:** HW Export from Vivado GUI creates another path as default workspace.
  - The build images are located in the "<plnx-proj-root>/images/linux" directory
6. Configure the **boot.scr** file as needed, see [Distro Boot with Boot.scr](#)<sup>11</sup>
7. Copy PetaLinux build image files to prebuilt folder
  - copy **u-boot.elf**, **u-boot.dtb**, **system.dtb**, **bl31.elf**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder

 "<project folder>\prebuilt\os\petalinux\<ddr size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

8. Generate Programming Files with Vitis

**run on Vivado TCL (Script generates applications and bootable files, which are defined in "test\_board\sw\_lib\apps\_list.csv")**

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start with TE
Scripts on Vivado TCL)
```

 TCL scripts generate also platform project, this must be done manually in case GUI is used. See [Vitis](#)<sup>12</sup>

<sup>9</sup> <https://wiki.trenz-electronic.de/display/PD/Vivado+Board+Part+Flow>

<sup>10</sup> <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>

<sup>11</sup> <https://wiki.trenz-electronic.de/display/PD/Distro+Boot+with+Boot.scr>


<sup>12</sup> <https://wiki.trenz-electronic.de/display/PD/Vitis>



## 6 Launch

For basic board setup, LEDs... see: [TEBF0808 Getting Started](#)<sup>13</sup>


### 6.1 Programming

 Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging](#)<sup>14</sup>

#### 6.1.1 Get prebuilt boot binaries

1. Run `_create_win_setup.cmd/_create_linux_setup.sh` and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
  - a. Select assembly version
  - b. Validate selection
  - c. Select create and open delivery binary folder

 Note: Folder "<project folder>\\_binaries\_<Article Name>" with subfolder "boot\_<app name>" for different applications will be generated

#### 6.1.2 QSPI-Boot mode

Option for **Boot.bin** on QSPI Flash.

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado\_open\_existing\_project\_gui mode.cmd" or if not created, create with "vivado\_create\_project\_gui mode.cmd"

**run on Vivado TCL (Script programs BOOT.bin on QSPI flash)**

```
TE::pr_program_flash -swapp hello_te0808
```

3. Set Boot Mode to **QSPI-Boot**
  - Depends on Carrier, see carrier TRM.
  - TEBF0808 change automatically the Boot Mode to SD, if SD is inserted, optional CPLD Firmware without Boot Mode changing for microSD Slot is available on the download area

#### 6.1.3 SD-Boot mode

1. Copy **image.ub**, **boot.scr** and **Boot.bin** on **SD**
  - use files from "<project folder>\\_binaries\_<Article Name>\boot\_linux" from generated binary folder, see: [Get prebuilt boot binaries](#)(see page 25)
  - or use prebuilt file location, see "<project folder>\prebuilt\file\_location.txt"
2. Set Boot Mode to SD-Boot.

<sup>13</sup> <https://wiki.trenz-electronic.de/display/PD/TEBF0808+Getting+Started>

<sup>14</sup> <https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDDevelopmentTools-XilinxSoftwareProgrammingandDebugging>


- Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.


### 6.1.4 JTAG

Not used on this Example.

## 6.2 Usage

1. Prepare HW like described on section [Programming](#)(see page 25)
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)

 Note: See TRM of the Carrier, which is used.

 Starting with Petalinux version 2020.1, the industry standard "Distro-Boot" boot flow for U-Boot was introduced, which significantly expands the possibilities of the boot process and has the primary goal of making booting much more standardised and predictable. The boot options described above describe the common boot processes for this hardware; other boot options are possible. For more information see [Distro Boot with Boot.scr](#)<sup>15</sup>

4. (Optional with TEBF0808) Insert PCIe Card (detection depends on Linux driver. Only some basic drivers are installed)
5. (Optional with TEBF0808) Connect SATA Disc
6. (Optional with TEBF0808) Connect Display Port Monitor (List of usable Monitors: <https://www.xilinx.com/support/answers/68671.html>)
7. (Optional with TEBF0808) Connect Network Cable
8. Power On PCB

#### **boot process**

1. ZynqMP Boot ROM loads FSBL from SD/QSPI into OCM,
2. FSBL init the PS, programs the PL using the bitstream and loads PMU, ATF and U-boot from SD/QSPI into DDR,
3. U-boot loads Linux (**image.ub**) from SD/QSPI/... into DDR

### 6.2.1 Linux

1. Open Serial Console (e.g. putty)
  - Speed: 115200
  - select COM Port


 Win OS, see device manager, Linux OS see dmesg |grep tty (UART is \*USB1)

2. Linux Console:

```
# password default disabled with 2021.2 petalinux release
```

<sup>15</sup> <https://wiki.trenz-electronic.de/display/PD/Distro+Boot+with+Boot.scr>

```
petalinux login: root
Password: root
```

 Note: Wait until Linux boot finished

3. You can use Linux shell now.

```
i2cdetect -y -r 0    (check I2C 0 Bus, replace 0 with other bus number is
also possible)
dmesg | grep rtc     (RTC check)
udhcpc              (ETH0 check)
lsusb               (USB check)
lspci               (PCIe check)
```

4. Option Features

- Webserver to get access to ZynqMP
  - insert IP on web browser to start web interface
- init.sh scripts
  - add init.sh script on SD, content will be load automatically on startup (template included in "<project folder>\misc\SD")

## 6.2.2 Vivado Hardware Manager

Open Vivado HW-Manager and add VIO signal to dashboard (\*.ltx located on prebuilt folder).

- RGPIO Interface (**Important:** CPLD Firmware REV07 or newer is needed) for Control and Monitoring:
  - Set Enable to send Write data over RGPIO interface.
    - **Important use CPLD Firmware REV07 or newer:** <https://wiki.trenz-electronic.de/display/PD/TEBF0808+CPLD>
      - Buttons, LEDs, Status...
- Control:
  - LEDs: XMOD 2 (without green dot) and HD LED are accessible.
  - CAN\_S

hw\_vios

hw\_vio\_1

hw\_vio\_2

Q

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Dashboard Options

Name

Value

Acti...

Directi...

VIO

↳ zsysw_iRGPIOMio_rgpio_s_enable	[B] 1	▼	Output	hw_vio_1
> ↳ zsysw_iRGPIOMio_rgpio_s_23dt12_PG[11:0]	[H] FFF		Input	hw_vio_1
> ↳ zsysw_iRGPIOMio_rgpio_s_23dt8_unused[15:0]	[H] 0000	▼	Output	hw_vio_1
> ↳ zsysw_iRGPIOMio_rgpio_s_11dt8_bootmode[3:0]	[H] 5		Input	hw_vio_1
> ↳ zsysw_iRGPIOMio_rgpio_s_7dt6_ER_ERST[1:0]	[H] 0		Input	hw_vio_1
> ↳ zsysw_iRGPIOMio_rgpio_s_7dt0_data[7:0]	[H] 1F	▼	Output	hw_vio_1
> ↳ zsysw_iRGPIOMio_rgpio_s_6dt5_SD_CD[1:0]	[H] 1		Input	hw_vio_1
↳ zsysw_iRGPIOMio_rgpio_s_3_unused	[B] 1		Input	hw_vio_1
↳ zsysw_iRGPIOMio_rgpio_s_2_xmod1_button	[B] 1		Input	hw_vio_1
↳ zsysw_iRGPIOMio_rgpio_s_1_S5_2_bootmode	[B] 0		Input	hw_vio_1
↳ zsysw_iRGPIOMio_rgpio_s_0_S5_1_bootmode	[B] 0		Input	hw_vio_1
↳ zsysw_iRGPIOMio_rgpio_m_enable	[B] 1	▼	Output	hw_vio_1
> ↳ zsysw_iRGPIOMio_rgpio_m_23dt12_unused[11:0]	[H] 000	▼	Output	hw_vio_1
↳ zsysw_iRGPIOMio_rgpio_m_23_PJTAG_SRST	[B] 1		Input	hw_vio_1
↳ zsysw_iRGPIOMio_rgpio_m_22_PJTAG_TRST	[B] 1		Input	hw_vio_1
↳ zsysw_iRGPIOMio_rgpio_m_21_FMC_CLKDIR	[B] 0		Input	hw_vio_1
↳ zsysw_iRGPIOMio_rgpio_m_20_SD_WP	[B] 0		Input	hw_vio_1
↳ zsysw_iRGPIOMio_rgpio_m_19_reserved	[B] 0		Input	hw_vio_1
↳ zsysw_iRGPIOMio_rgpio_m_18_S5_4_FMCVADJ	[B] 1		Input	hw_vio_1
↳ zsysw_iRGPIOMio_rgpio_m_17_S5_3_USER	[B] 1		Input	hw_vio_1
↳ zsysw_iRGPIOMio_rgpio_m_16_XMOD2BUTTON	[B] 1		Input	hw_vio_1
> ↳ zsysw_iRGPIOMio_rgpio_m_15dt13_PHY_LEDS[2:0]	[H] 7		Input	hw_vio_1
↳ zsysw_iRGPIOMio_rgpio_m_12_CAN_FAULT	[B] 0		Input	hw_vio_1
> ↳ zsysw_iRGPIOMio_rgpio_m_11dt8_muxsel[3:0]	[H] 0	▼	Output	hw_vio_1
> ↳ zsysw_iRGPIOMio_rgpio_m_11dt8_MUX[3:0]	[H] 0		Input	hw_vio_1
> ↳ zsysw_iRGPIOMio_rgpio_m_7dt6_unused[1:0]	[H] 0	▼	Output	hw_vio_1
> ↳ zsysw_iRGPIOMio_rgpio_m_7dt0_data[7:0]	[H] 1F		Input	hw_vio_1
> ↳ zsysw_iRGPIOMio_rgpio_m_5dt0_leds[5:0]	[H] 00	▼	Output	hw_vio_1

hw\_vios

hw\_vio\_1

hw\_vio\_2

Q

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Dashboard Options

Name

Value

Acti...

Directi...

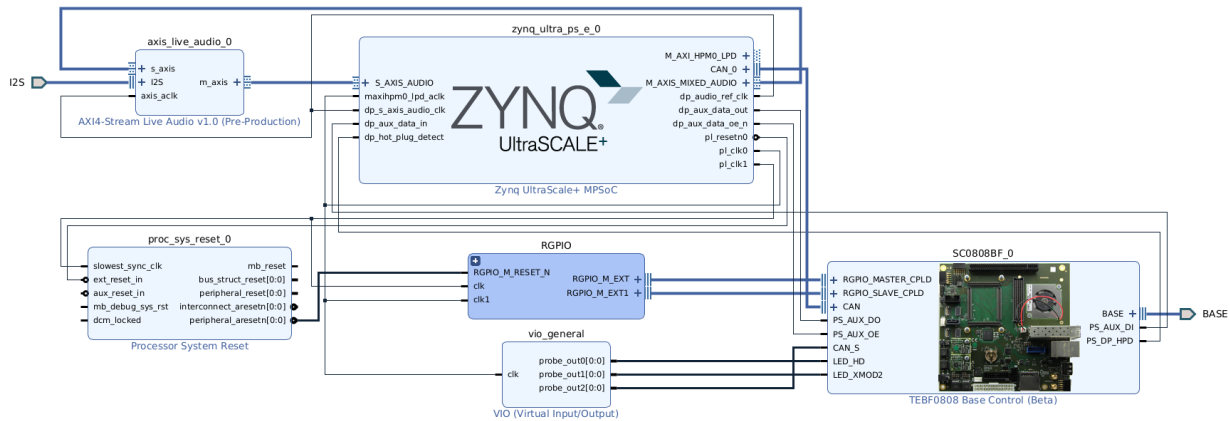
VIO

↳ zsysw_iWio_CAN_0_S	[B] 0	▼	Output	hw_vio_2
↳ zsysw_iWio_LED_HD	[B] 0	▼	Output	hw_vio_2
↳ zsysw_iWio_LED_XMOD2	[B] 0	▼	Output	hw_vio_2

### Table 10: Vivado Hardware Manager

## 7 System Design - Vivado

### 7.1 Block Design



**Figure 1: Block Design**

#### 7.1.1 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
CAN0	EMIO
I2C0	MIO
PJTAG0	MIO
UART0	MIO

Type	Note
GPIO0	MIO
SWDT0..1	
TTC0..3	
GEM3	MIO
USB0	MIO/GTP
PCIe	MIO/GTP
SATA	GTP
Display Port	EMIO/GTP

**Table 11: PS Interfaces**

## 7.2 Constrains

### 7.2.1 Basic module constrains

#### **\_i\_bitgen.xdc**

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

### 7.2.2 Design specific constrain

#### **\_i\_io.xdc**

```
#System Controller IP
#LED_HD SC0 J3:31
#LED_XMOD SC17 J3:48
#CAN RX SC19 J3:52 B47_L2_P in
#CAN TX SC18 J3:50 B47_L2_N out
#CAN S SC16 J3:46 B47_L3_N out
#HDIO_SC1 K14
#HDIO_SC2 H13
```

```

#HDIO_SC3      H14
#HDIO_SC4      F13

#HDIO_SC0      J14
set_property PACKAGE_PIN J14 [get_ports BASE_sc0]
#HDIO_SC5      G13
set_property PACKAGE_PIN G13 [get_ports BASE_sc5]
#HDIO_SC6      J15
set_property PACKAGE_PIN J15 [get_ports BASE_sc6]
#HDIO_SC7      K15
set_property PACKAGE_PIN K15 [get_ports BASE_sc7]
#HDIO_SC10     A15
set_property PACKAGE_PIN A15 [get_ports BASE_sc10_io]
#HDIO_SC11     B15
set_property PACKAGE_PIN B15 [get_ports BASE_sc11]
#HDIO_SC12     C13
set_property PACKAGE_PIN C13 [get_ports BASE_sc12]
#HDIO_SC13     C14
set_property PACKAGE_PIN C14 [get_ports BASE_sc13]
#HDIO_SC14     E13
set_property PACKAGE_PIN E13 [get_ports BASE_sc14]
#HDIO_SC15     E14
set_property PACKAGE_PIN E14 [get_ports BASE_sc15]
#HDIO_SC16     A13
set_property PACKAGE_PIN A13 [get_ports BASE_sc16]
#HDIO_SC17     B13
set_property PACKAGE_PIN B13 [get_ports BASE_sc17]
#HDIO_SC18     A14
set_property PACKAGE_PIN A14 [get_ports BASE_sc18]
#HDIO_SC19     B14
set_property PACKAGE_PIN B14 [get_ports BASE_sc19]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc0]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc5]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc6]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc7]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc10_io]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc11]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc12]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc13]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc14]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc15]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc16]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc17]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc18]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc19]

# Audio Codec
#LRCLK          J3:49 B47_L9_N
#BCLK           J3:51 B47_L9_P
#DAC_SDATA     J3:53 B47_L7_N
#ADC_SDATA     J3:55 B47_L7_P

#LRCLK G14

```

```
set_property PACKAGE_PIN G14 [get_ports I2S_lrclk ]  
#BCLK G15  
set_property PACKAGE_PIN G15 [get_ports I2S_bclk ]  
#DAC_SDATA E15  
set_property PACKAGE_PIN E15 [get_ports I2S_sdin ]  
#ADC_SDATA F15  
set_property PACKAGE_PIN F15 [get_ports I2S_sdout ]  
set_property IOSTANDARD LVCMOS18 [get_ports I2S_lrclk ]  
set_property IOSTANDARD LVCMOS18 [get_ports I2S_bclk ]  
set_property IOSTANDARD LVCMOS18 [get_ports I2S_sdin ]  
set_property IOSTANDARD LVCMOS18 [get_ports I2S_sdout ]
```



## 8 Software Design - Vitis

---

For Vitis project creation, follow instructions from:

[Vitis](#)<sup>16</sup>

### 8.1 Application

---

Template location: "<project folder>\sw\_lib\sw\_apps\"

#### 8.1.1 zynqmp\_fsbl

---

TE modified 2021.2 FSBL

General:

- Modified Files: xfsbl\_main.c, xfsbl\_hooks.h/.c, xfsbl\_board.h/.c (search for 'TE Mod' on source code)
- Add Files: te\_xfsbl\_hooks.h/.c (for hooks and board)
- General Changes:
  - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te\_\*
  - Si5345 Configuration
  - OTG+PCIe Reset over MIO
  - I2C MUX for EEPROM MAC

#### 8.1.2 zynqmp\_pmufw

---

Xilinx default PMU firmware.

#### 8.1.3 hello\_te0808

---

Hello TE0808 is a Xilinx Hello World example as endless loop instead of one console output.

#### 8.1.4 u-boot

---

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

---

<sup>16</sup> <https://wiki.trenz-electronic.de/display/PD/Vitis>

## 9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- [PetaLinux KICKstart](#)<sup>17</sup>

### 9.1 Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- select SD default instead of eMMC:
  - CONFIG\_SUBSYSTEM\_PRIMARY\_SD\_PSU\_SD\_1\_SELECT=y
- generate u-boot.dtb:
  - CONFIG\_SUBSYSTEM\_UBOOT\_EXT\_DTB=y
- add new flash partition for bootscr and sizing
  - CONFIG\_SUBSYSTEM\_FLASH\_PSU\_QSPI\_0\_BANKLESS\_PART0\_SIZE=0xA00000
  - CONFIG\_SUBSYSTEM\_FLASH\_PSU\_QSPI\_0\_BANKLESS\_PART2\_SIZE=0x2000000
  - CONFIG\_SUBSYSTEM\_FLASH\_PSU\_QSPI\_0\_BANKLESS\_PART3\_NAME="bootscr"
  - CONFIG\_SUBSYSTEM\_FLASH\_PSU\_QSPI\_0\_BANKLESS\_PART3\_SIZE=0x80000

### 9.2 U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- MAC from eeprom together with uboot and device tree settings:
  - CONFIG\_ZYNQ\_GEM\_I2C\_MAC\_OFFSET=0xFA
  - CONFIG\_ENV\_OVERWRITE=y
  - CONFIG\_SYS\_I2C\_EEPROM\_ADDR=0x50
  - CONFIG\_SYS\_I2C\_EEPROM\_BUS=7
- Boot Modes:
  - CONFIG\_QSPI\_BOOT=y
  - CONFIG\_SD\_BOOT=y
  - # CONFIG\_ENV\_IS\_IN\_NAND is not set
  - CONFIG\_BOOT\_SCRIPT\_OFFSET=0x2A40000

Change platform-top.h:

```
#no changes
```

### 9.3 Device Tree

**project-spec\meta-user\recipes-bsp\device-tree\files\system-user.dtsi**

```
/include/ "system-conf.dtsi"
/ {
```

<sup>17</sup> <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>

```

    chosen {
        xlnx,eeeprom = &eeeprom;
    };
};

/*----- gtr -----*/

//https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/18841716/
//Zynq+Ultrascale+MPSOC+Linux+SIU+driver

/ {
    refclk3:psgtr_dp_clock {
        compatible = "fixed-clock";
        #clock-cells = <0x00>;
        clock-frequency = <27000000>;
    };

    refclk2:psgtr_pcie_usb_clock {
        compatible = "fixed-clock";
        #clock-cells = <0x00>;
        clock-frequency = <100000000>;
    };

    refclk1:psgtr_sata_clock {
        compatible = "fixed-clock";
        #clock-cells = <0x00>;
        clock-frequency = <150000000>;
    };

    //refclk0:psgtr_unused_clock {
    //    compatible = "fixed-clock";
    //    #clock-cells = <0x00>;
    //    clock-frequency = <100000000>;
    //};
};

&psgtr {
    clocks = <&refclk1 &refclk2 &refclk3>;
    /* ref clk instances used per lane */
    clock-names = "ref1\0ref2\0ref3";
};

/*----- SD -----*/
&sdhci0 {
    // disable-wp;
    no-1-8-v;
};

&sdhci1 {
    // disable-wp;
    no-1-8-v;
};

```

```

};

/*----- USB -----*/
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    snps,usb3_lpm_capable;
    snps,dis_u3_susphy_quirk;
    snps,dis_u2_susphy_quirk;
    phy-names = "usb2-phy","usb3-phy";
    maximum-speed = "super-speed";
};

/*----- ETH PHY -----*/
&gem3 {
    phy-handle = <&phy0>;
    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>;
    };
};

/*----- QSPI -----*/
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};

/*----- I2C -----*/
&i2c0 {
    i2cswitch@73 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x73>;
        i2c-mux-idle-disconnect;
        i2c@0 { // MCLK TEBF0808 SI5338A, 570FBB000290DG_unassembled
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <0>;
        };
        i2c@1 { // SFP TEBF0808 PCF8574DWR
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <1>;
        };
    };
};

```

```

};
i2c@2 { // PCIe
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <2>;
};
i2c@3 { // SFP1 TEBF0808
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <3>;
};
i2c@4 { // SFP2 TEBF0808
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <4>;
};
i2c@5 { // TEBF0808 EEPROM
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <5>;
    eeprom: eeprom@50 {
        compatible = "atmel,24c08";
        reg = <0x50>;
    };
};
i2c@6 { // TEBF0808 FMC
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <6>;
};
i2c@7 { // TEBF0808 USB HUB
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <7>;
};
};
i2cswitch@77 { // u
    compatible = "nxp,pca9548";
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <0x77>;
    i2c-mux-idle-disconnect;
    i2c@0 { // TEBF0808 PMOD P1
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0>;
    };
};
i2c@1 { // i2c Audio Codec
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <1>;
    /*
    adau1761: adau1761@38 {
        compatible = "adi,adau1761";
        reg = <0x38>;
    };
    */
};

```

```

        */
    };
    i2c@2 { // TEBF0808 Firefly A
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <2>;
    };
    i2c@3 { // TEBF0808 Firefly B
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <3>;
    };
    i2c@4 { //Module PLL Si5338 or SI5345
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <4>;
    };
    i2c@5 { //TEBF0808 CPLD
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <5>;
    };
    i2c@6 { //TEBF0808 Firefly PCF8574DWR
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <6>;
    };
    i2c@7 { // TEBF0808 PMOD P3
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <7>;
    };
};
};

```

#### project-spec\meta-user\recipes-bsp\uboot-device-tree\files\system-user.dtsi

```

/include/ "system-conf.dtsi"
/ {
    chosen {
        xlnx,eeeprom = &eeeprom;
    };
};

/*----- gtr -----*/

//https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/18841716/
//Zynq+Ultrascale+MPSOC+Linux+SIU+driver

/ {
    refclk3:psgtr_dp_clock {
        compatible = "fixed-clock";
    };
};

```

```

        #clock-cells = <0x00>;
        clock-frequency = <27000000>;
    };

    refclk2:psgtr_pcie_usb_clock {
        compatible = "fixed-clock";
        #clock-cells = <0x00>;
        clock-frequency = <100000000>;
    };

    refclk1:psgtr_sata_clock {
        compatible = "fixed-clock";
        #clock-cells = <0x00>;
        clock-frequency = <150000000>;
    };

    //refclk0:psgtr_unused_clock {
    //    compatible = "fixed-clock";
    //    #clock-cells = <0x00>;
    //    clock-frequency = <100000000>;
    //};
};

&psgtr {
    clocks = <&refclk1 &refclk2 &refclk3>;
    /* ref clk instances used per lane */
    clock-names = "ref1\0ref2\0ref3";
};

/*----- SD -----*/
&sdhci0 {
    // disable-wp;
    no-1-8-v;
};

&sdhci1 {
    // disable-wp;
    no-1-8-v;
};

/*----- USB -----*/
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    snps,usb3_lpm_capable;
    snps,dis_u3_susphy_quirk;
    snps,dis_u2_susphy_quirk;
    phy-names = "usb2-phy","usb3-phy";
    maximum-speed = "super-speed";
};

```

```

/*----- ETH PHY -----*/
&gem3 {
    phy-handle = <&phy0>;
    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>;
    };
};

/*----- QSPI -----*/
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};

/*----- I2C -----*/
&i2c0 {
    i2cswitch@73 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x73>;
        i2c-mux-idle-disconnect;
        i2c@0 { // MCLK TEBF0808 SI5338A, 570FBB000290DG_unassembled
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <0>;
        };
        i2c@1 { // SFP TEBF0808 PCF8574DWR
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <1>;
        };
        i2c@2 { // PCIE
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <2>;
        };
        i2c@3 { // SFP1 TEBF0808
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <3>;
        };
        i2c@4 { // SFP2 TEBF0808
            #address-cells = <1>;
            #size-cells = <0>;

```



```

        reg = <4>;
    };
    i2c@5 { // TEBF0808 EEPROM
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <5>;
        eeprom: eeprom@50 {
            compatible = "atmel,24c08";
            reg = <0x50>;
        };
    };
    i2c@6 { // TEBF0808 FMC
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <6>;
    };
    i2c@7 { // TEBF0808 USB HUB
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <7>;
    };
};
i2cswitch@77 { // u
    compatible = "nxp,pca9548";
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <0x77>;
    i2c-mux-idle-disconnect;
    i2c@0 { // TEBF0808 PMOD P1
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0>;
    };
    i2c@1 { // i2c Audio Codec
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <1>;
        /*
        adau1761: adau1761@38 {
            compatible = "adi,adau1761";
            reg = <0x38>;
        };
        */
    };
    i2c@2 { // TEBF0808 Firefly A
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <2>;
    };
    i2c@3 { // TEBF0808 Firefly B
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <3>;
    };
    i2c@4 { //Module PLL Si5338 or SI5345
        #address-cells = <1>;

```

```

        #size-cells = <0>;
        reg = <4>;
    };
    i2c@5 { //TEBF0808 CPLD
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <5>;
    };
    i2c@6 { //TEBF0808 Firefly PCF8574DWR
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <6>;
    };
    i2c@7 { // TEBF0808 PMOD P3
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <7>;
    };
};
};
};

```

## 9.4 FSBL patch

Must be add manually, see template

## 9.5 Kernel

Start with **petalinux-config -c kernel**

Changes:

- Only needed to fix JTAG Debug issue:
  - # CONFIG\_CPU\_IDLE is not set
  - # CONFIG\_CPU\_FREQ is not set
  - CONFIG\_EDAC\_CORTEX\_ARM64=y
- Support PCIe memory card
  - CONFIG\_NVME\_CORE=y
  - CONFIG\_BLK\_DEV\_NVME=y
  - # CONFIG\_NVME\_MULTIPATH is not set
  - # CONFIG\_NVME\_HWMON is not set
  - # CONFIG\_NVME\_TCP is not set
  - CONFIG\_NVME\_TARGET=y
  - # CONFIG\_NVME\_TARGET\_PASSTHRU is not set
  - # CONFIG\_NVME\_TARGET\_LOOP is not set
  - # CONFIG\_NVME\_TARGET\_FC is not set
  - # CONFIG\_NVME\_TARGET\_TCP is not set
  - CONFIG\_SATA\_AHCI=y
  - CONFIG\_SATA\_MOBILE\_LPM\_POLICY=0
  - CONFIG\_NVM=y
  - CONFIG\_NVM\_PBLK=y
  - CONFIG\_NVM\_PBLK\_DEBUG=y

## 9.6 Rootfs

---

Start with **petalinux-config -c rootfs**

Changes:

- For web server app:
  - CONFIG\_busybox-httpd=y
- For additional test tools only:
  - CONFIG\_i2c-tools=y
  - CONFIG\_packagegroup-petalinux-utils=y (util-linux,cpufrequtils,bridge-utils,mtd-utils,usbutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)

## 9.7 Applications

---

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-apps\"

### 9.7.1 startup

---

Script App to load init.sh from SD Card if available.

### 9.7.2 webfwu

---

Webserver application suitable for ZynqMP access. Need busybox-httpd

## 10 Additional Software

---

### 10.1 SI5345

---

File location "<project folder>/misc/PLL/SI5345\_B/SI5345-\*.slabtimeproj"

General documentation how you work with these project will be available on [SI5345](https://wiki.trenz-electronic.de/display/PD/SI5345)<sup>18</sup>



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<sup>18</sup> <https://wiki.trenz-electronic.de/display/PD/SI5345>

## 11 Appx. A: Change History and Legal Notices

### 11.1 Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
 2023-04-13	v.55 (see page 6)	 @Manuela Strücker <sup>19</sup>	<ul style="list-style-type: none"> <li>script update</li> <li>new assembly variants</li> </ul>
2022-09-29	v.53	Manuela Strücker	<ul style="list-style-type: none"> <li>new assembly variants</li> </ul>
2022-09-29	v.51	Manuela Strücker	<ul style="list-style-type: none"> <li>update board part files compatible to Vivado 2021.2.1</li> </ul>
2022-09-06	v.50	Manuela Strücker	<ul style="list-style-type: none"> <li>typo</li> </ul>
2022-03.16	v.48	Manuela Strücker	<ul style="list-style-type: none"> <li>2021.2 release</li> <li>update board files</li> </ul>
2022-02-03	v.47	John Hartfiel	<ul style="list-style-type: none"> <li>Typo correction on key features section</li> </ul>
2021-07-15	v.46	Manuela Strücker	<ul style="list-style-type: none"> <li>Document Style update</li> </ul>
2021-05-12	v.44	John Hartfiel	<ul style="list-style-type: none"> <li>update board files</li> <li>update design</li> </ul>
2021-02-05	v.43	John Hartfiel	<ul style="list-style-type: none"> <li>2020.2 release</li> <li>document style update</li> </ul>
2020-11-06	v.41	John Hartfiel	<ul style="list-style-type: none"> <li>typo bugfix for programming part</li> </ul>
2020-09-29	v.40	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variants</li> </ul>

<sup>19</sup> <https://wiki.trenz-electronic.de/display/~m.struecker>

Date	Document Revision	Authors	Description
2020-03-25	v.37	John Hartfiel	<ul style="list-style-type: none"> <li>script update</li> </ul>
2020-02-25	v.35	John Hartfiel	<ul style="list-style-type: none"> <li>Update requirement section</li> </ul>
2020-01-23	v.34	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variants</li> <li>Release 2019.2</li> </ul>
2019-08-09	v.32	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variants</li> <li>small FSBL update</li> <li>minor document style update</li> </ul>
2019-05-07	v.29	John Hartfiel	<ul style="list-style-type: none"> <li>Release 2018.3</li> </ul>
2018-08-09	v.27	John Hartfiel	<ul style="list-style-type: none"> <li>Release 2018.2</li> </ul>
2018-05-25	v.21	John Hartfiel	<ul style="list-style-type: none"> <li>Solved known issues</li> </ul>
2018-04-30	v.19	John Hartfiel	<ul style="list-style-type: none"> <li>Update known issues</li> </ul>
2018-03-29	v.18	John Hartfiel	<ul style="list-style-type: none"> <li>New assembly variant</li> </ul>
2018-02-08	v.16	John Hartfiel	<ul style="list-style-type: none"> <li>Solved known issues</li> </ul>
2018-01-29	v.10	John Hartfiel	<ul style="list-style-type: none"> <li>Update known issues</li> </ul>
2018-01-18	v.8	John Hartfiel	<ul style="list-style-type: none"> <li>Update documentation only</li> </ul>
2018-01-17	v.7	John Hartfiel	<ul style="list-style-type: none"> <li>Update design</li> </ul>
2018-01-15	v.4	John Hartfiel	<ul style="list-style-type: none"> <li>Release 2017.4</li> </ul>
2017-12-20	v.2	John Hartfiel	<ul style="list-style-type: none"> <li>Release 2017.2</li> </ul>

Date	Document Revision	Authors	Description
	All	@ John Hartfiel <sup>20</sup> , Manuela Strücker <sup>21</sup>	

**Table 12: Document change history.**

## 11.2 Legal Notices

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### 11.3 Data Privacy

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Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

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<sup>20</sup> <https://wiki.trenz-electronic.de/display/~j.hartfiel>

<sup>21</sup> <https://wiki.trenz-electronic.de/display/~m.struecker>

## 11.7 Technology Licenses

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## 11.9 REACH, RoHS and WEEE

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Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.


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<sup>22</sup> <http://guidance.echa.europa.eu/>

<sup>23</sup> <https://echa.europa.eu/candidate-list-table>

<sup>24</sup> <http://www.echa.europa.eu/>



 2019-06-07